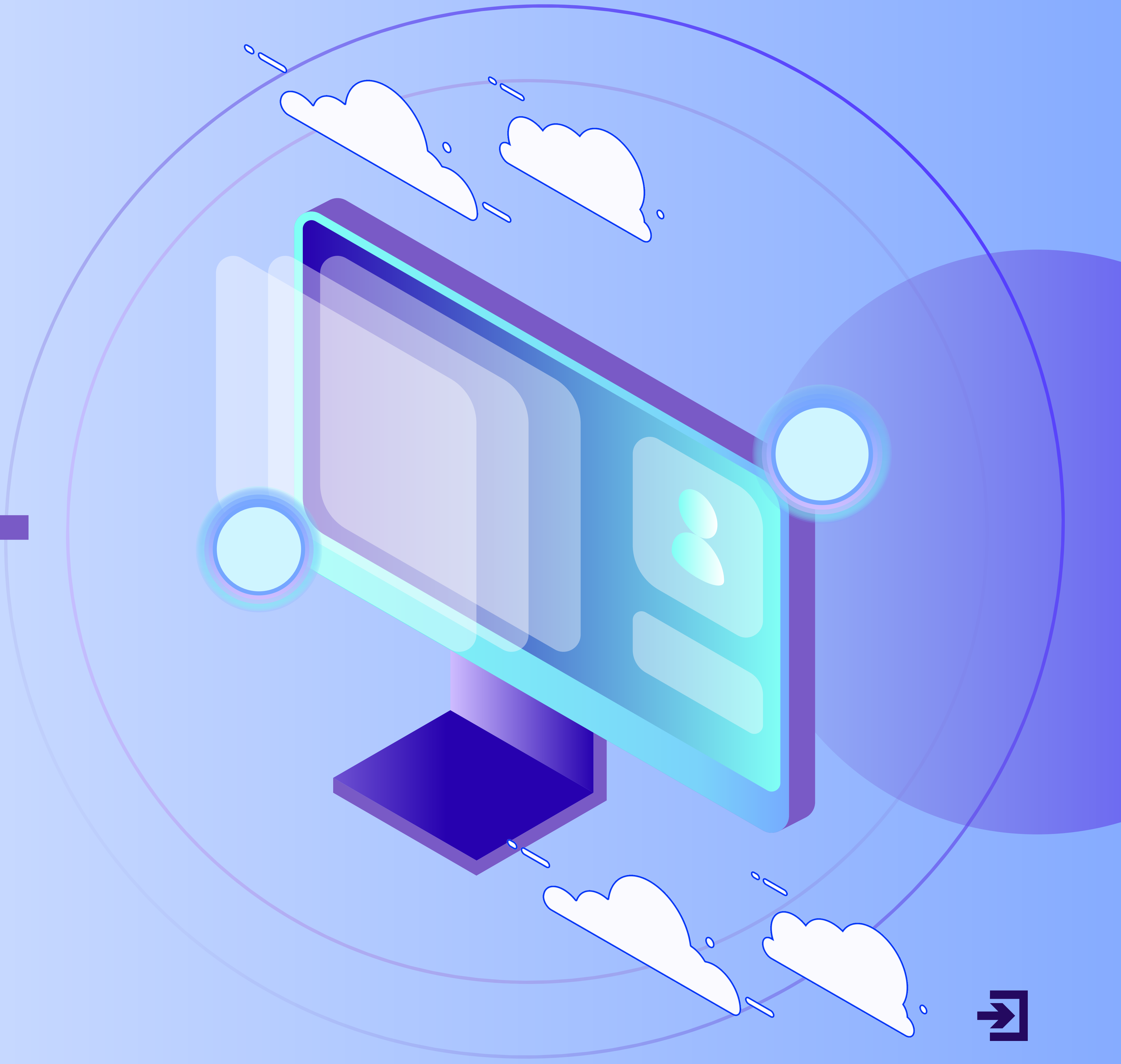
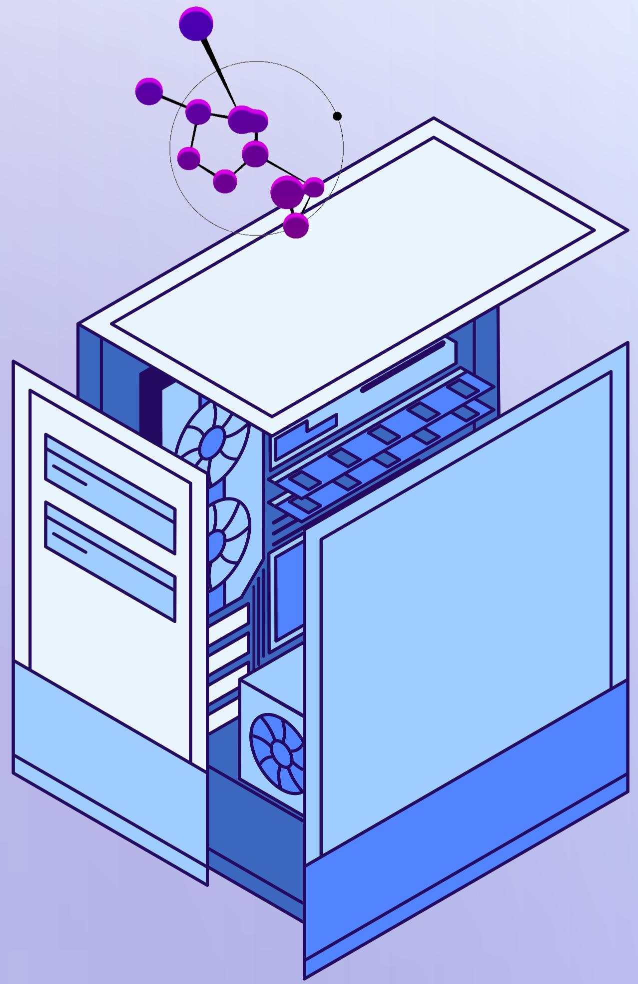
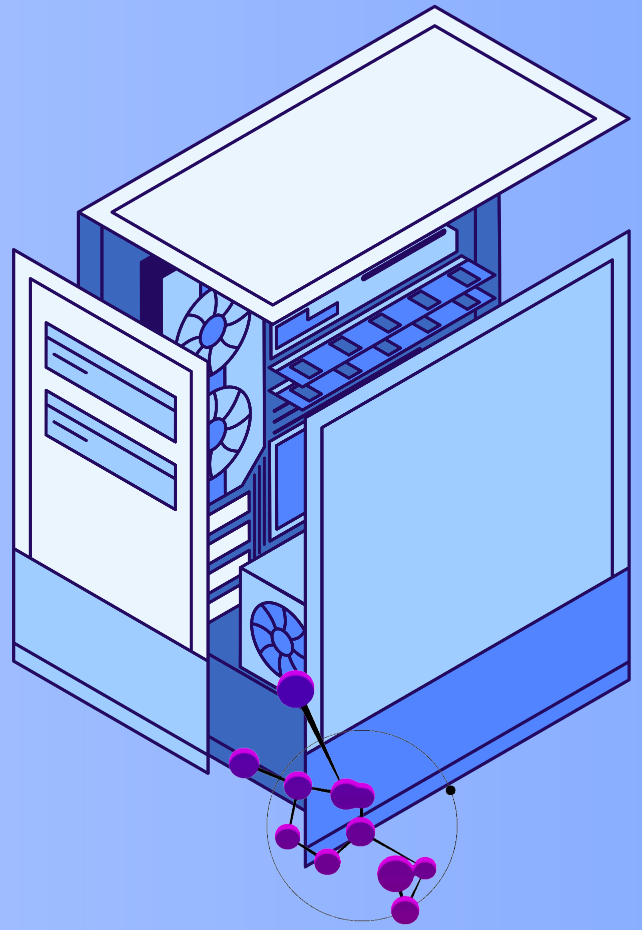
# DIGITAL LOGICAL
# DESIGN



# LAB PROJECT



## 4 BIT BINARY SYNCHRONOUS COUNTER



1. **Determine from the above description, the equations of T inputs for each T flip flop [...] in th[e] design of the counter.**

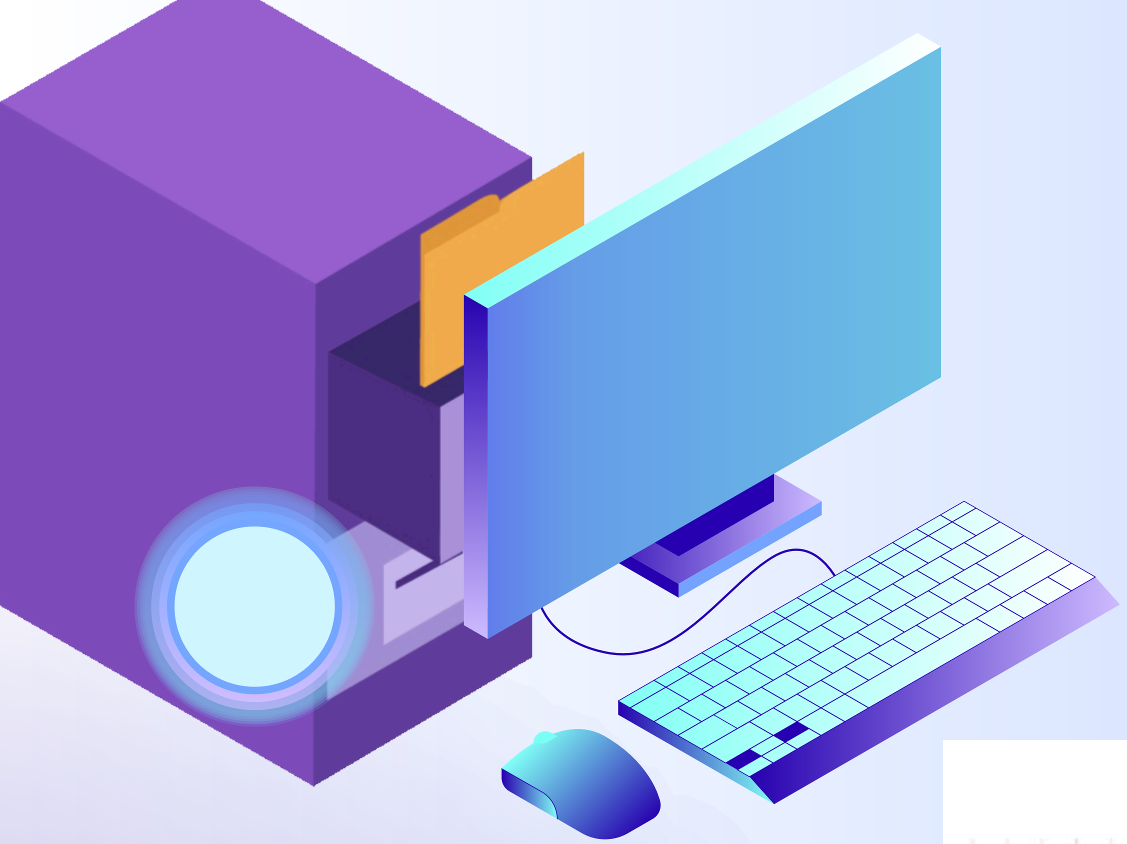
| Clock cycle | Q2 | Q1 | Q0 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 |
| 8 | 0 | 0 | 0 |

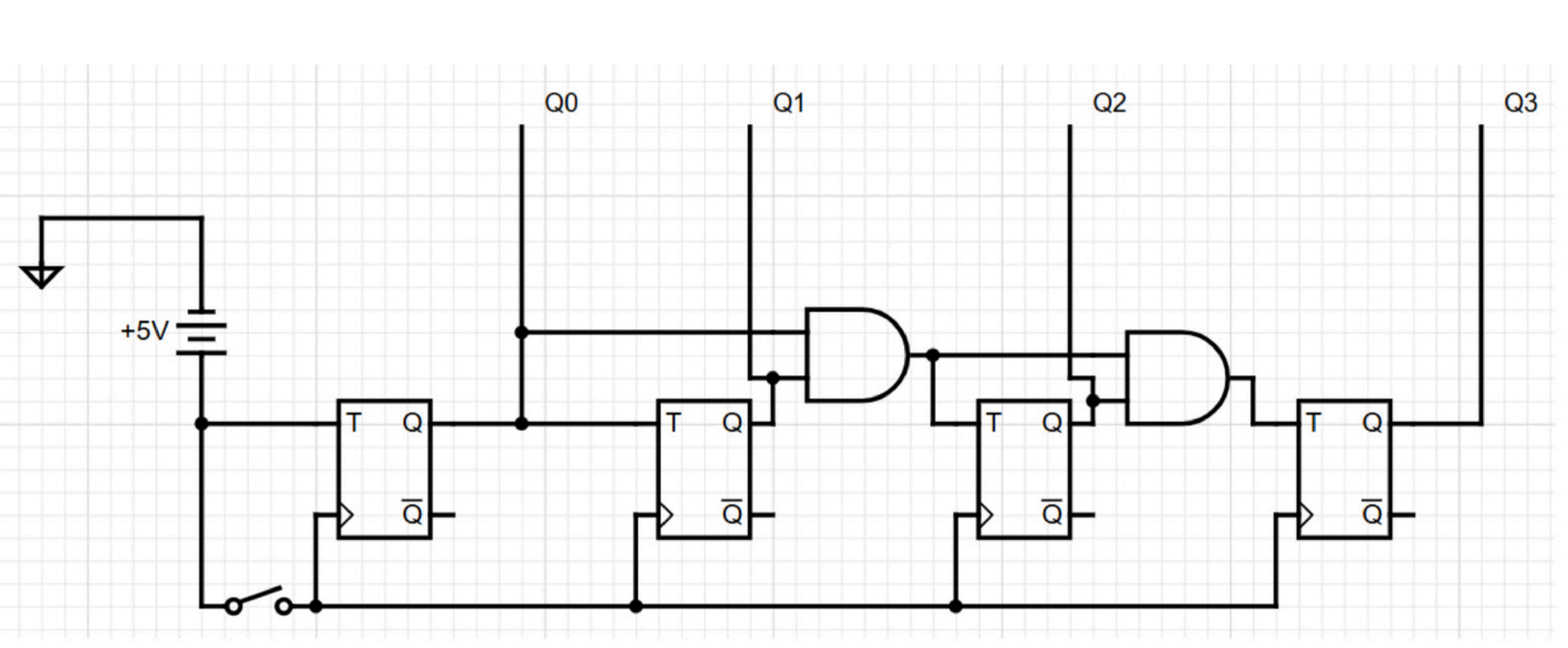
**1- T0 = 1: Q0 changes at every clock cycle, so T1 must always be 1**

**2- T1 = Q0: Q1 changes only when Q0 is 1, so T2 depends on Q0.**

**3- T2 = Q0 AND Q1: Q2 changes only when both Q0 and Q1 are 1, so T3 depends on their AND condition**

## 2. Design the circuit for a 4bit up-counter using T flip flop





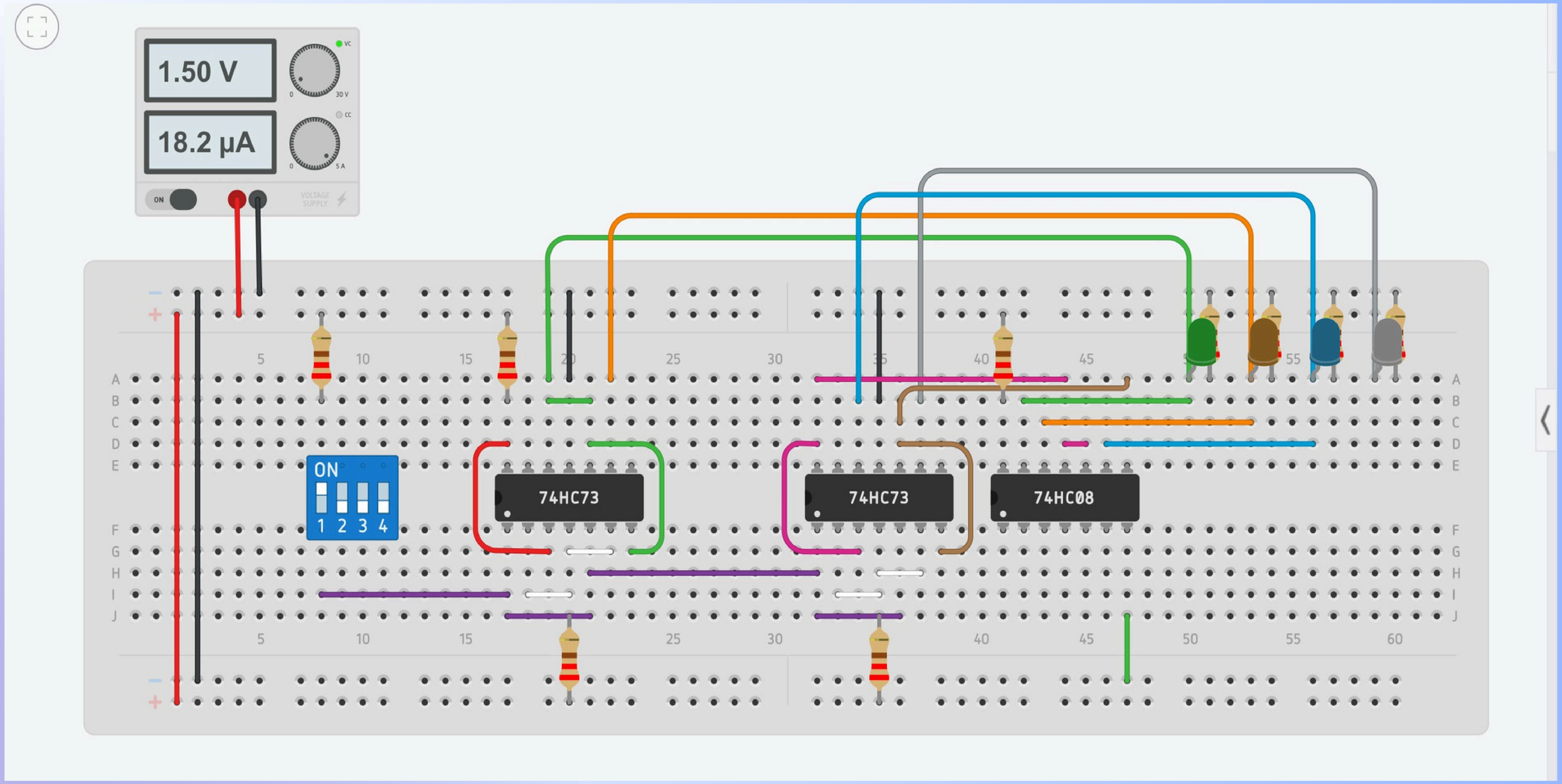
3. The equations of T inputs for each T flip flop used in the design of the counter.
The table below shows states every clock cycle.

| Clock Pulse | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ | Flip Notes |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | Initial state |
| 1 | 0 | 0 | 0 | 1 | $Q_0$ Flip |
| 2 | 0 | 0 | 1 | 0 | $Q_0$, $Q_1$ Flip |
| 3 | 0 | 0 | 1 | 1 | $Q_0$ Flip |
| 4 | 0 | 1 | 0 | 0 | $Q_0$, $Q_1$, $Q_2$ Flip |
| 5 | 0 | 1 | 0 | 1 | $Q_0$ Flip |
| 6 | 0 | 1 | 1 | 0 | $Q_0$, $Q_1$ Flip |
| 7 | 0 | 1 | 1 | 1 | $Q_0$ Flip |
| 8 | 1 | 0 | 0 | 0 | $Q_0$, $Q_1$, $Q_2$, $Q_3$ Flip |
| 9 | 1 | 0 | 0 | 1 | $Q_0$ Flip |
| 10 | 1 | 0 | 1 | 0 | $Q_0$, $Q_1$ Flip |
| 11 | 1 | 0 | 1 | 1 | $Q_0$ Flip |
| 12 | 1 | 1 | 0 | 0 | $Q_0$, $Q_1$, $Q_2$ Flip |
| 13 | 1 | 1 | 0 | 1 | $Q_0$ Flip |
| 14 | 1 | 1 | 1 | 0 | $Q_0$, $Q_1$ Flip |
| 15 | 1 | 1 | 1 | 1 | $Q_0$ Flip |
| 16 | 0 | 0 | 0 | 0 | Reset (All Flip) |

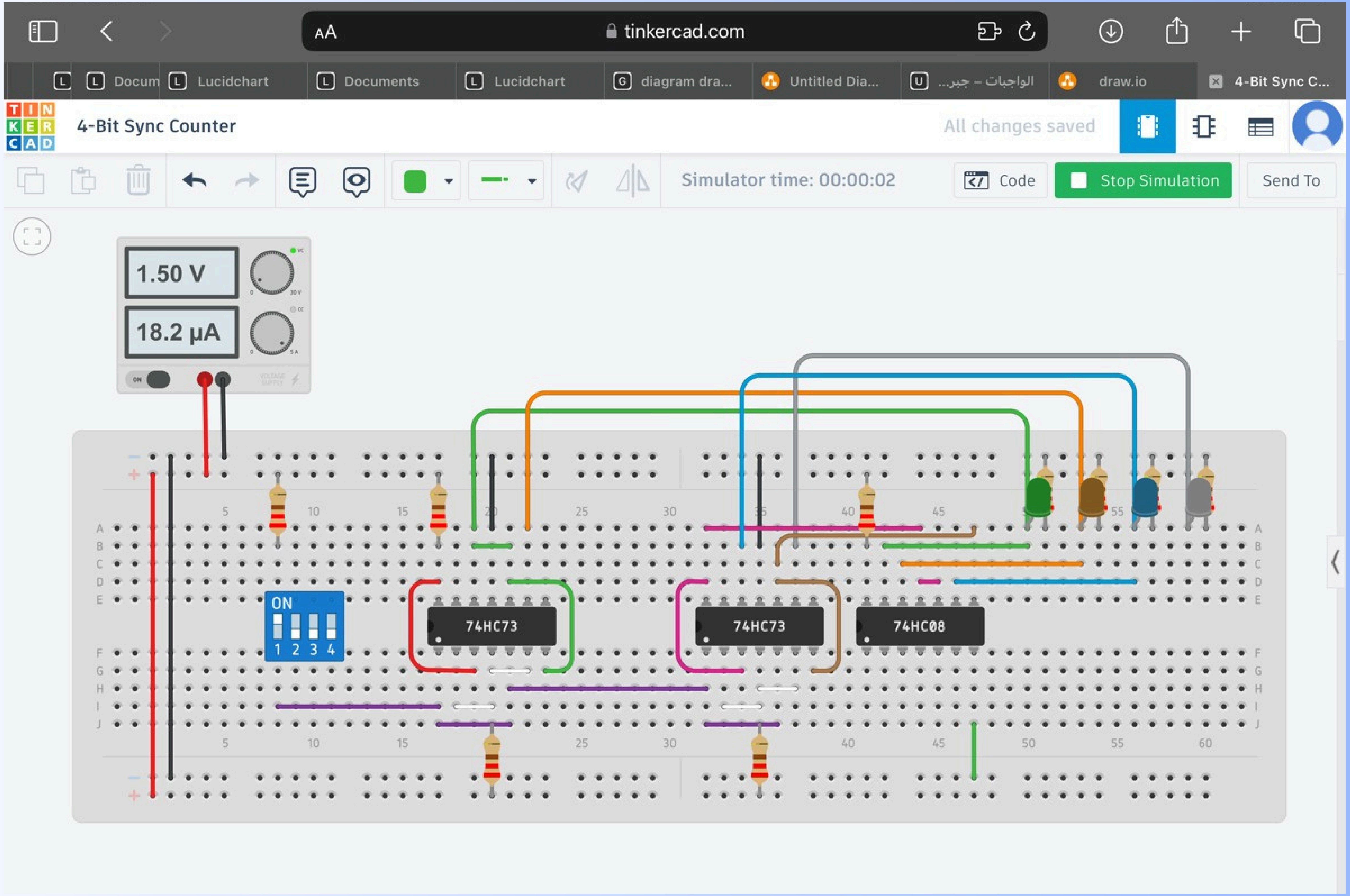
In a T flip-flop. The output flips on the (either falling or rising) edge of the clock, if T is set to 1.
∵ Q0 Flips on every cycle ∴T0 = 1
∵ Q1 Flips only if Q0 is set to 1 ∴T1 = Q0
∵ Q2 Flips only if Q0 and Q1 are set to 1 ∴T2 = Q0·Q1
∵ Q3 Flips only if Q0 and Q1 and Q2 are set to 1 ∴T3 = Q0·Q1·Q2

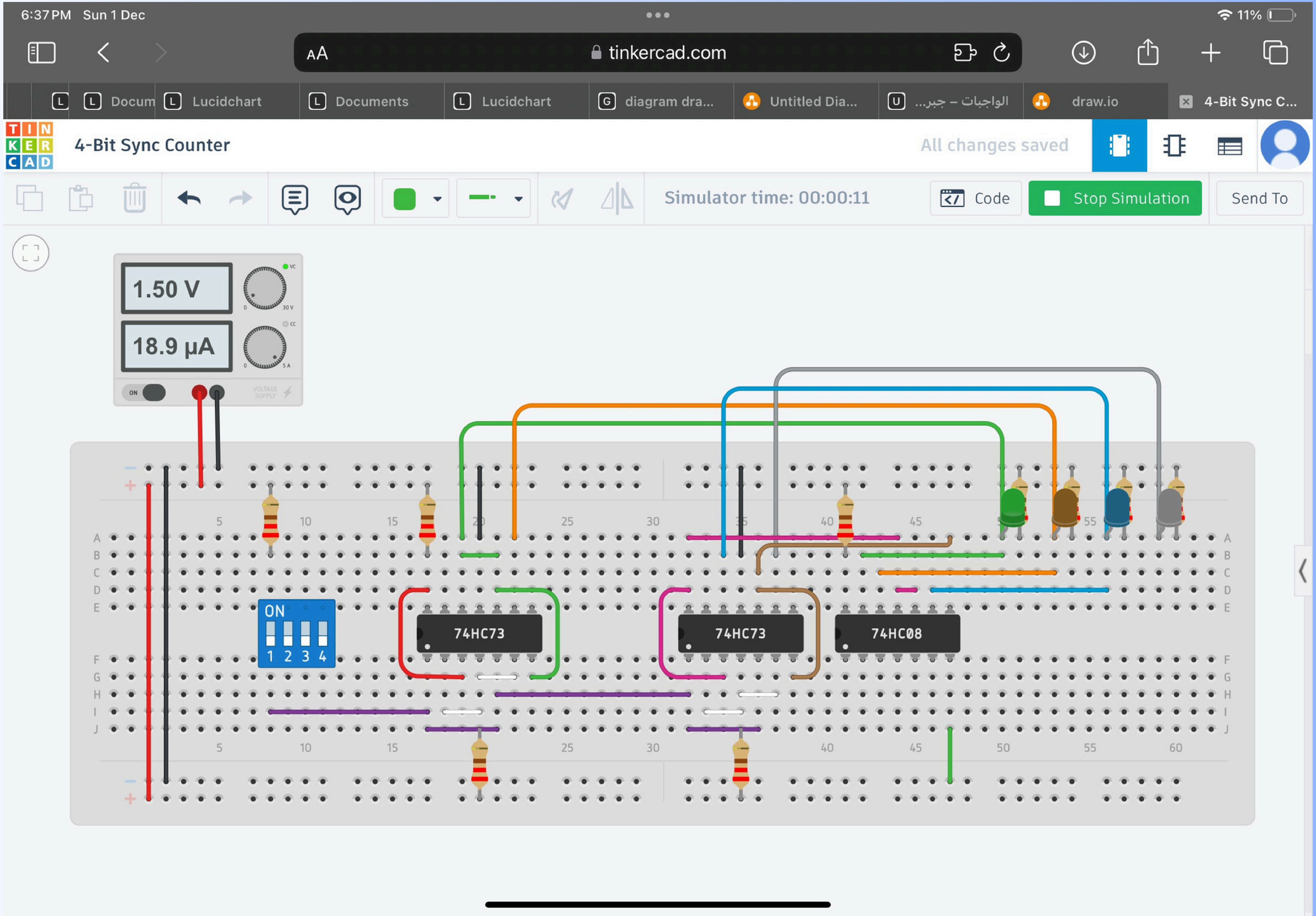
### 3. Implementation

A T flip-flop was implemented using a dual JK flip-flop IC by setting J, K both to T. Quad and IC 7408 was used to get the calculated
T values. Reset was disables by setting it to high. A DIP switch was used to feed the clock signa



# 4. Simulation

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Simulator time: 00:00:11
Code
Stop Simulation
Send To
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18.9 µA
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1 2 3 4
74HC73
74HC73
74HC08
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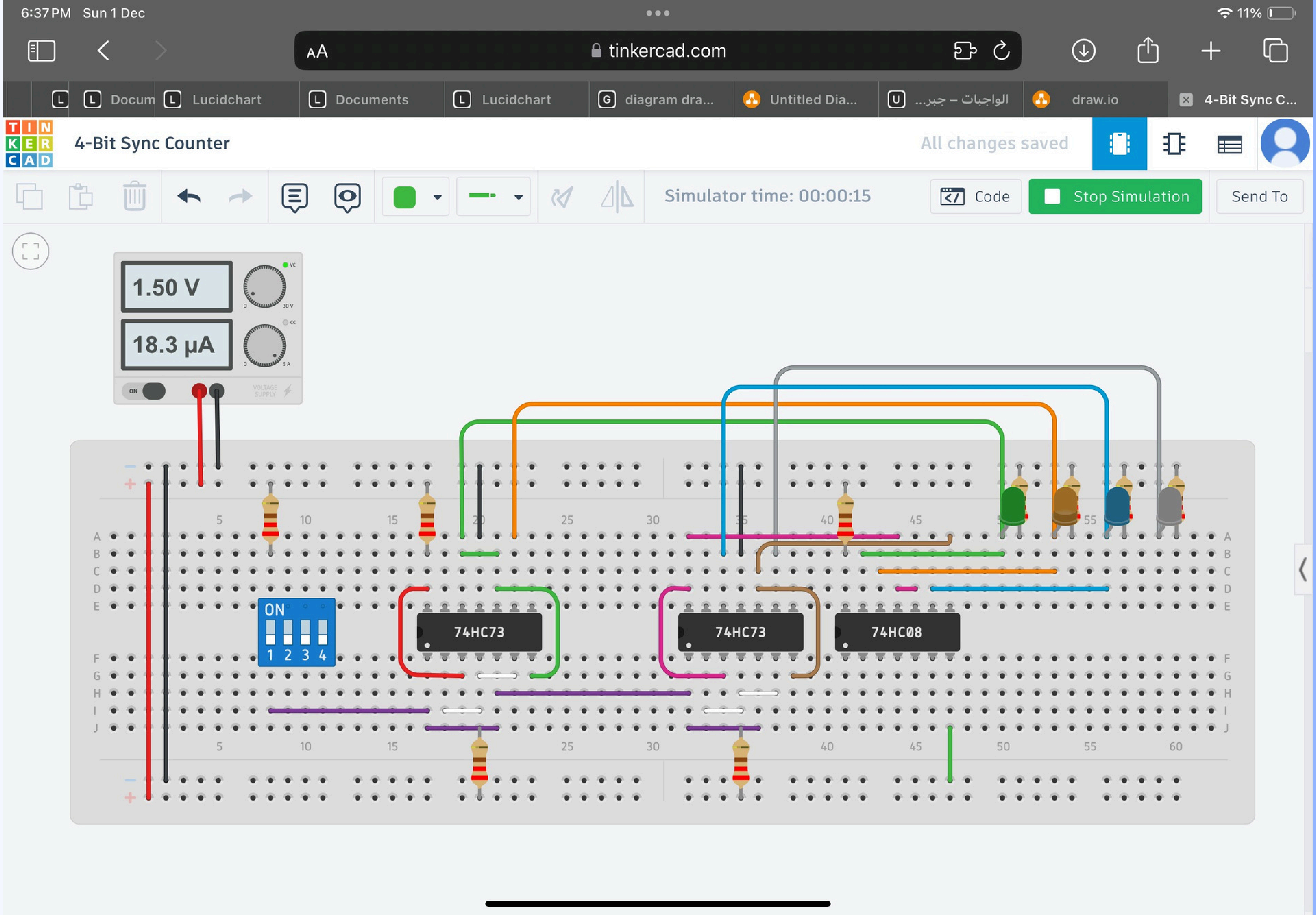
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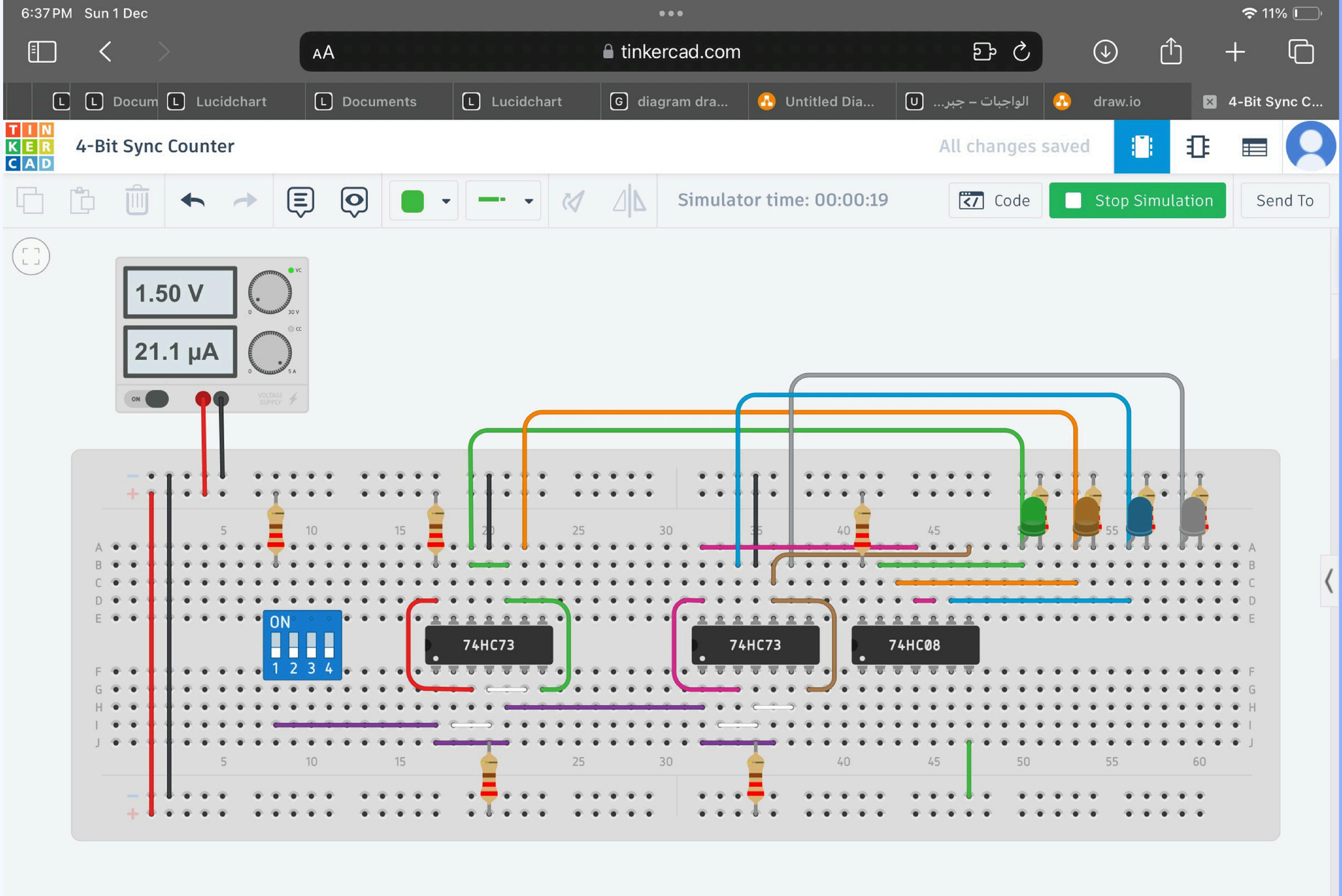
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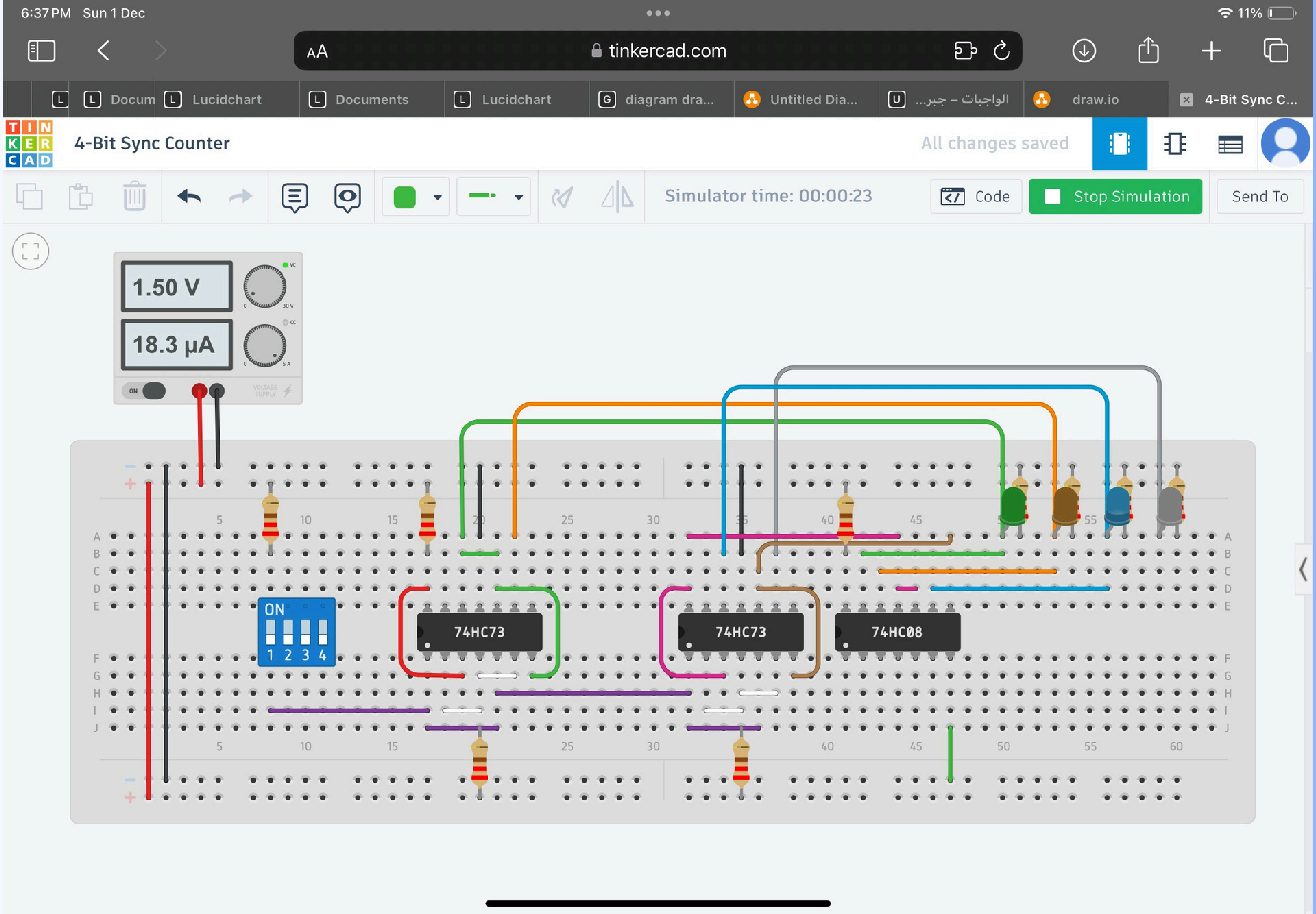
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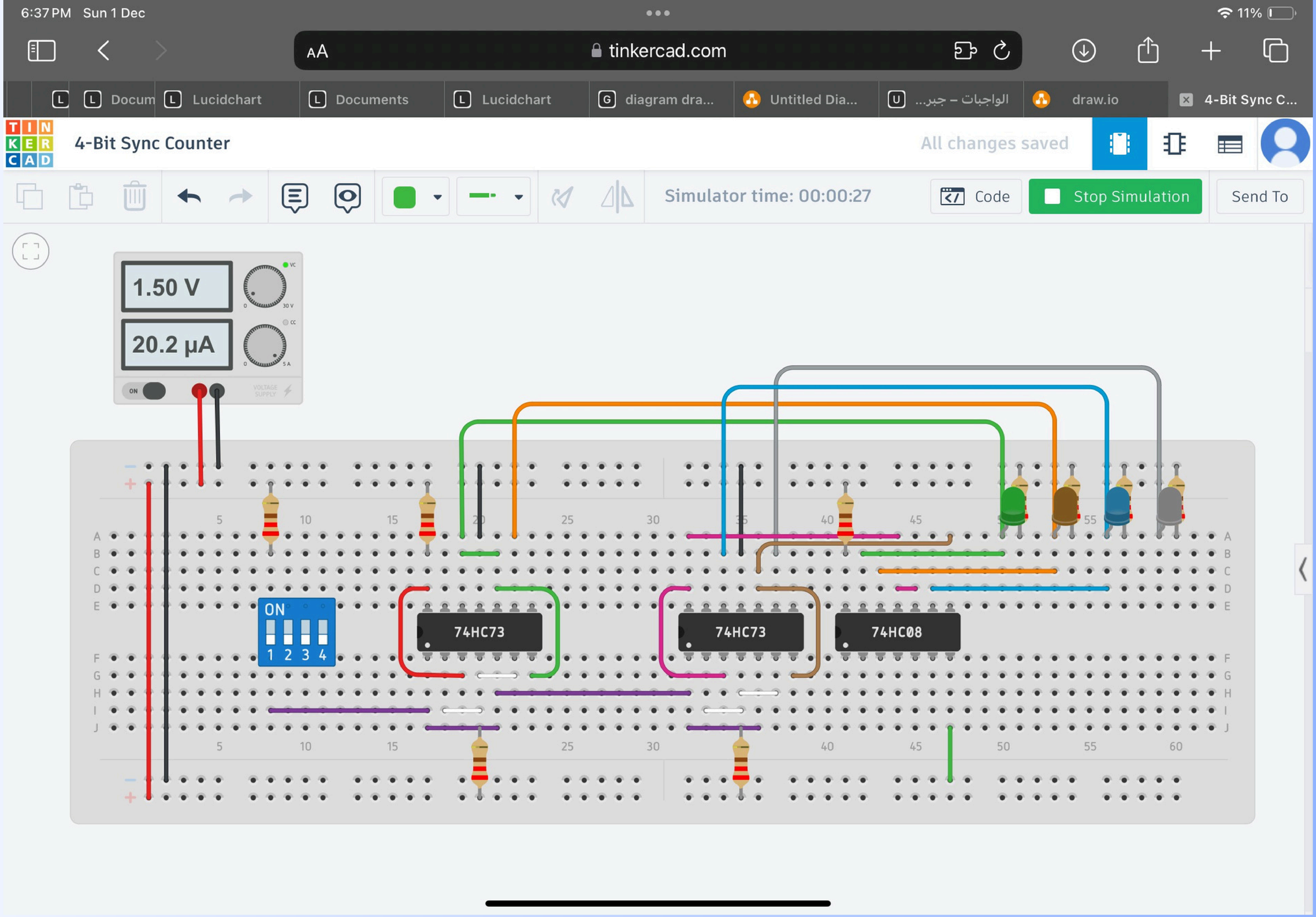
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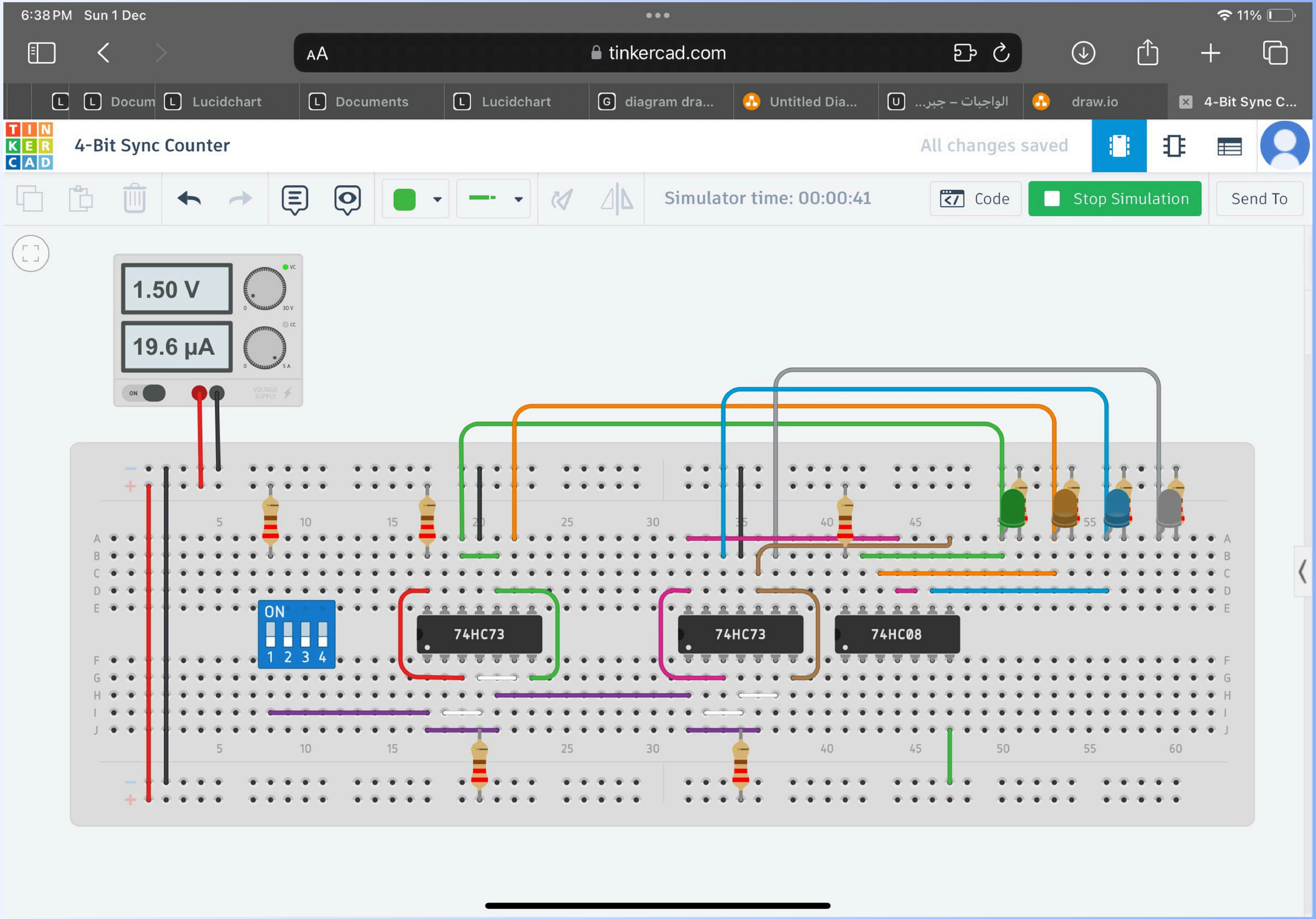
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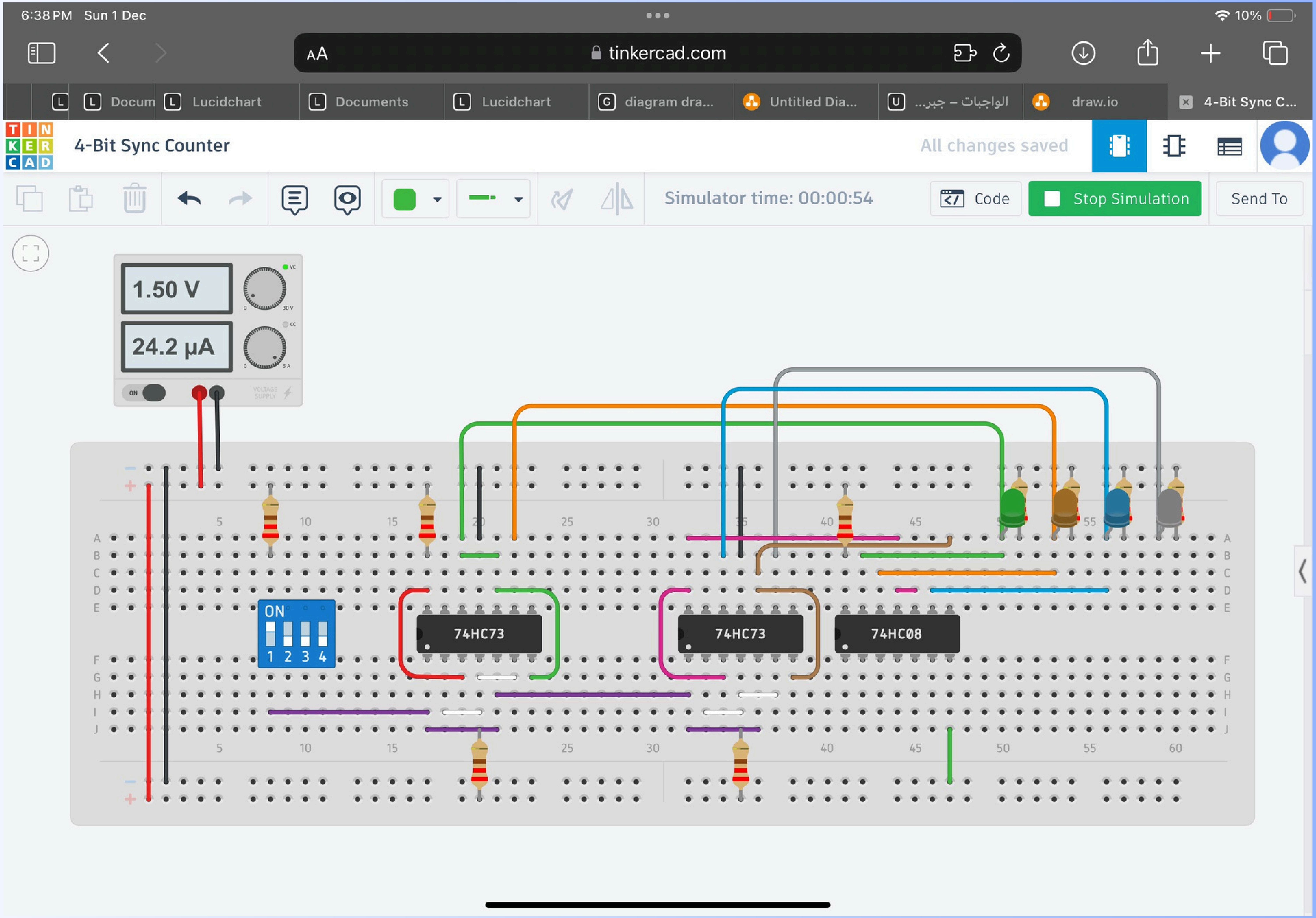

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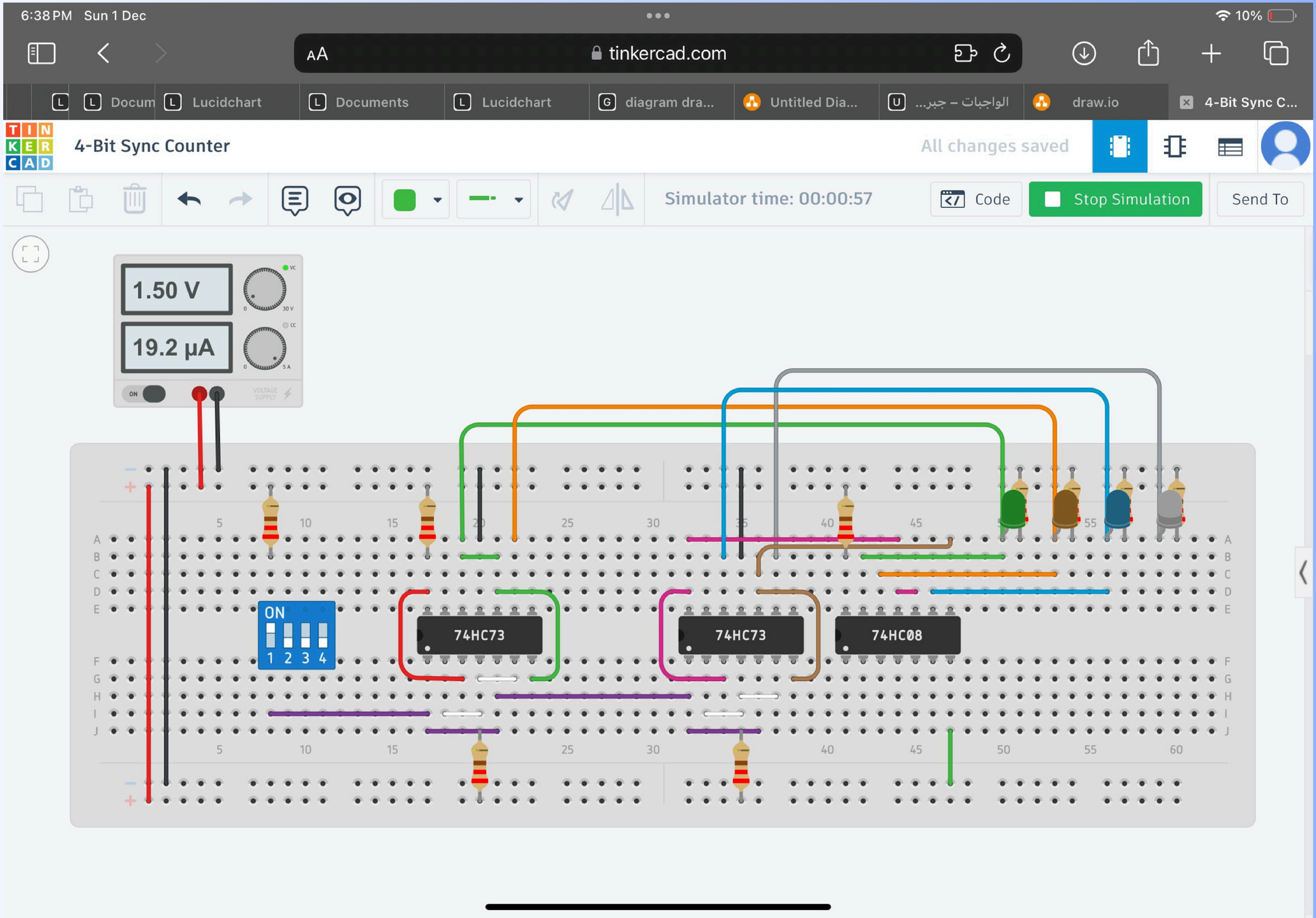

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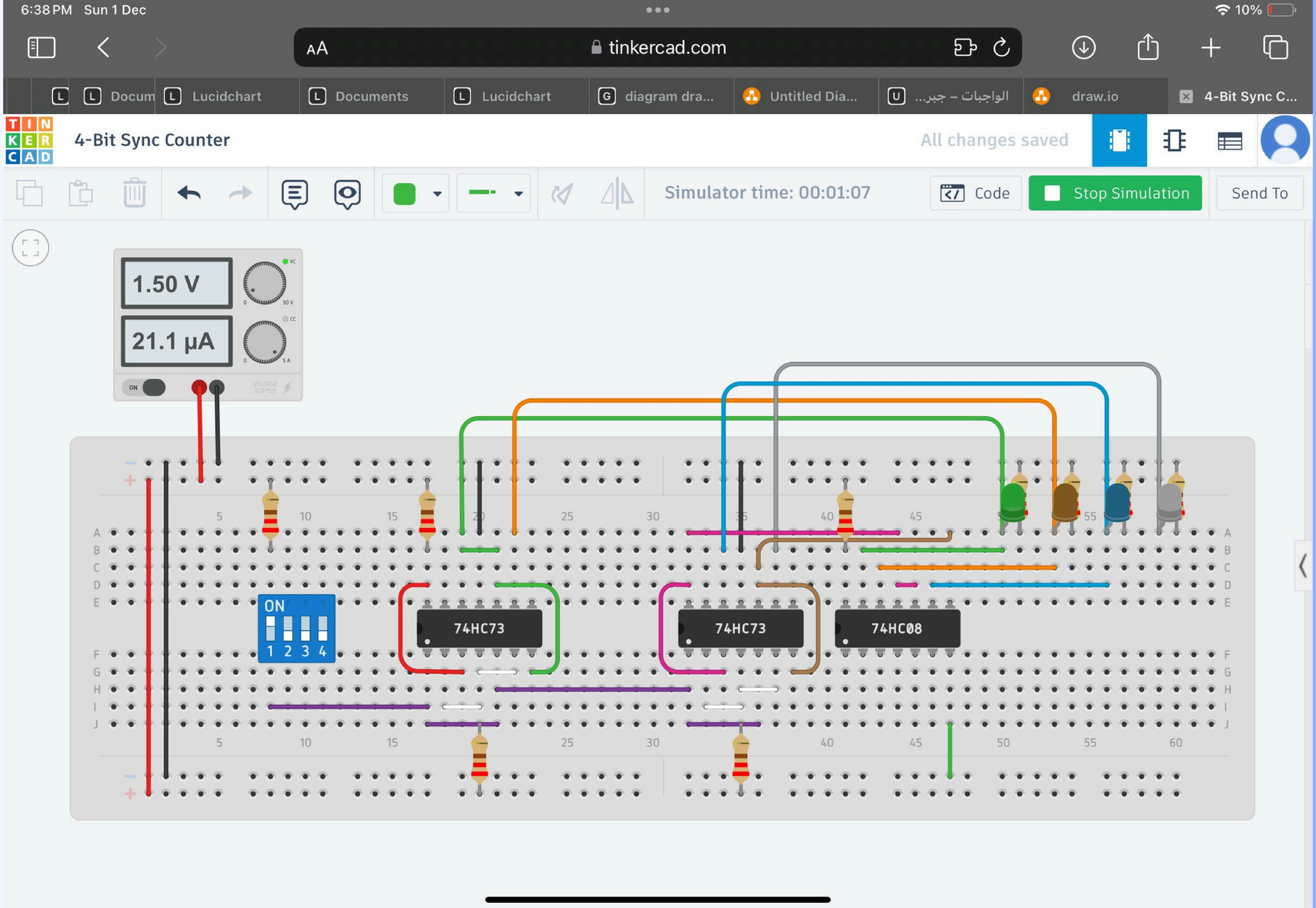
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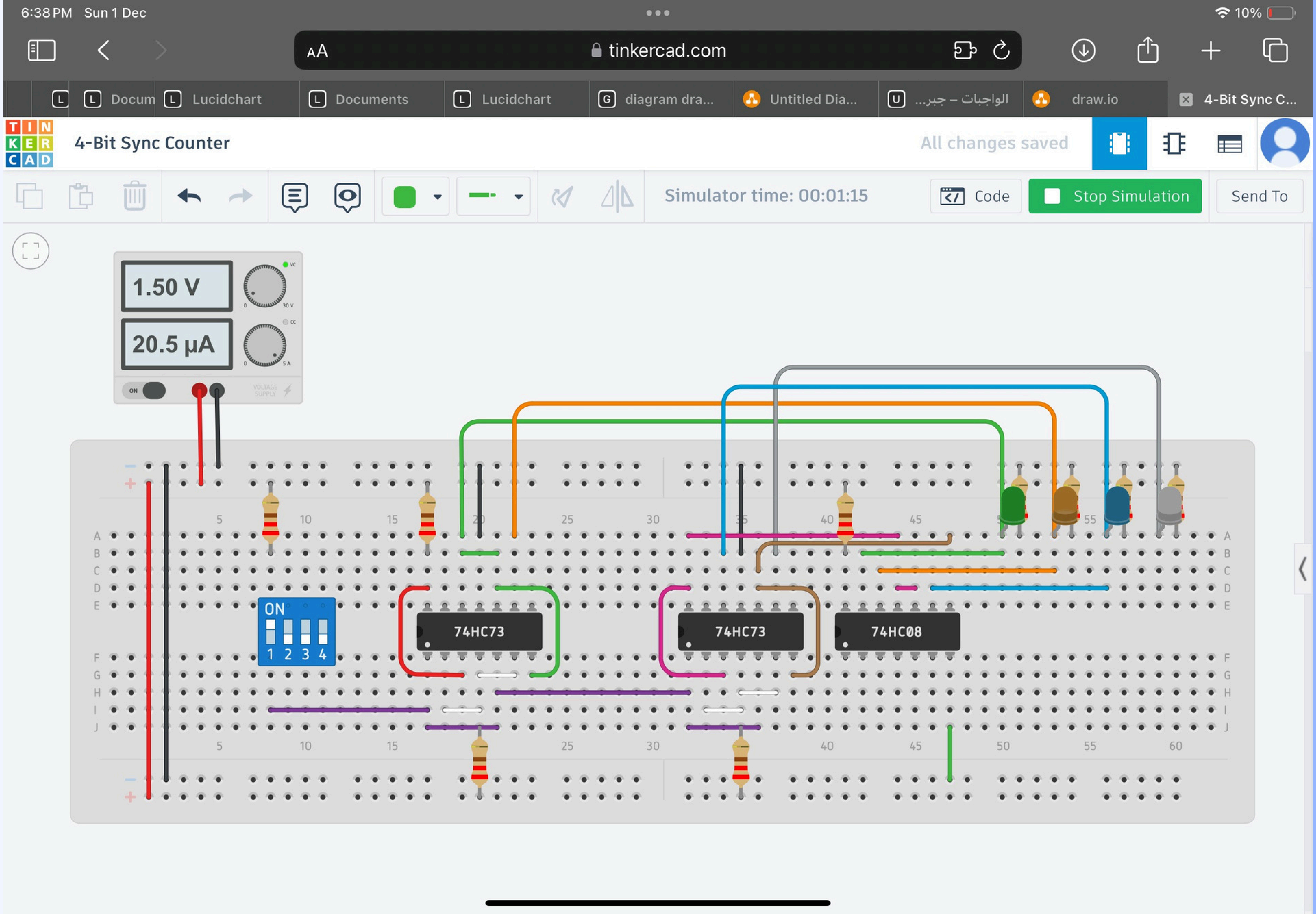
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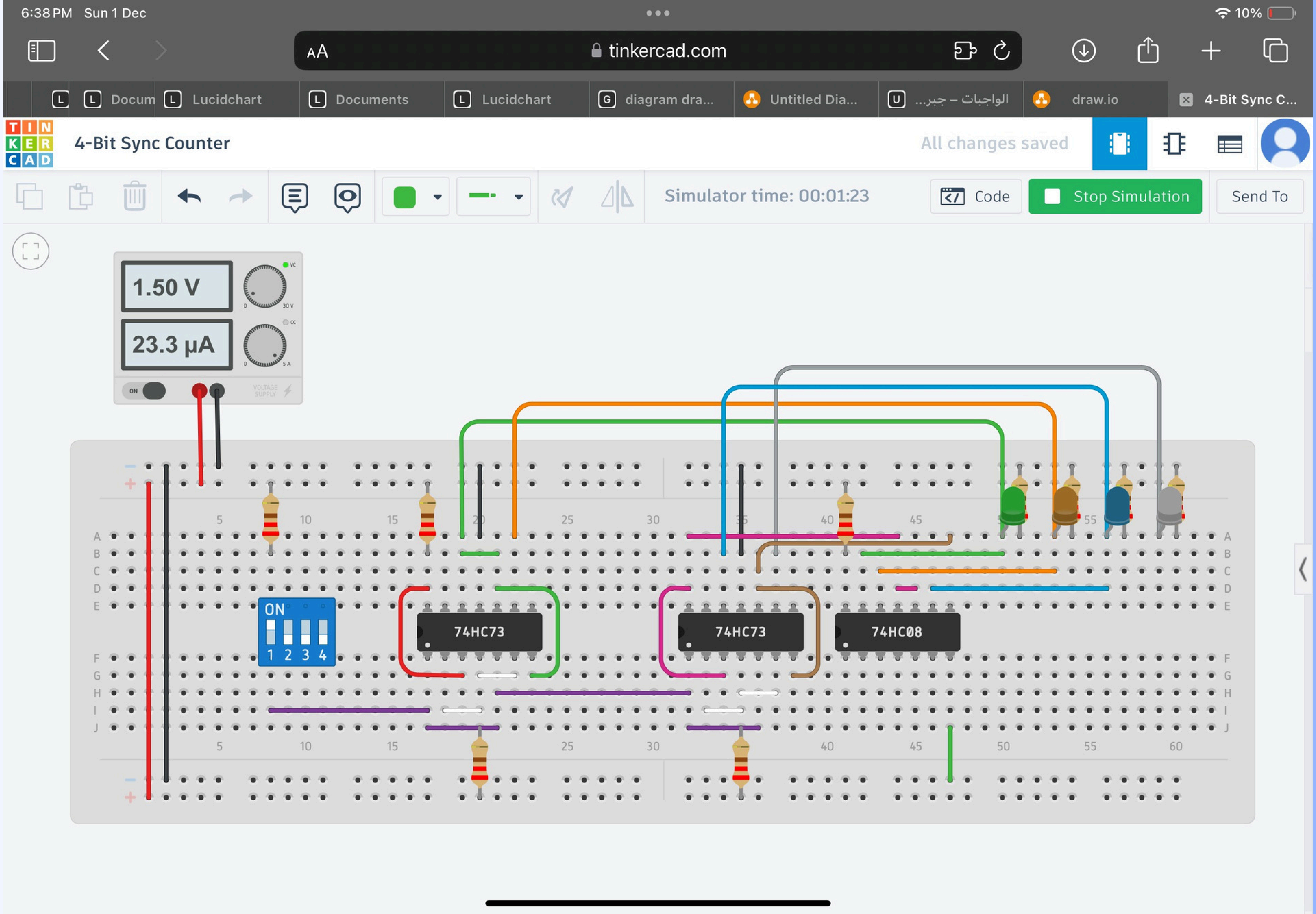
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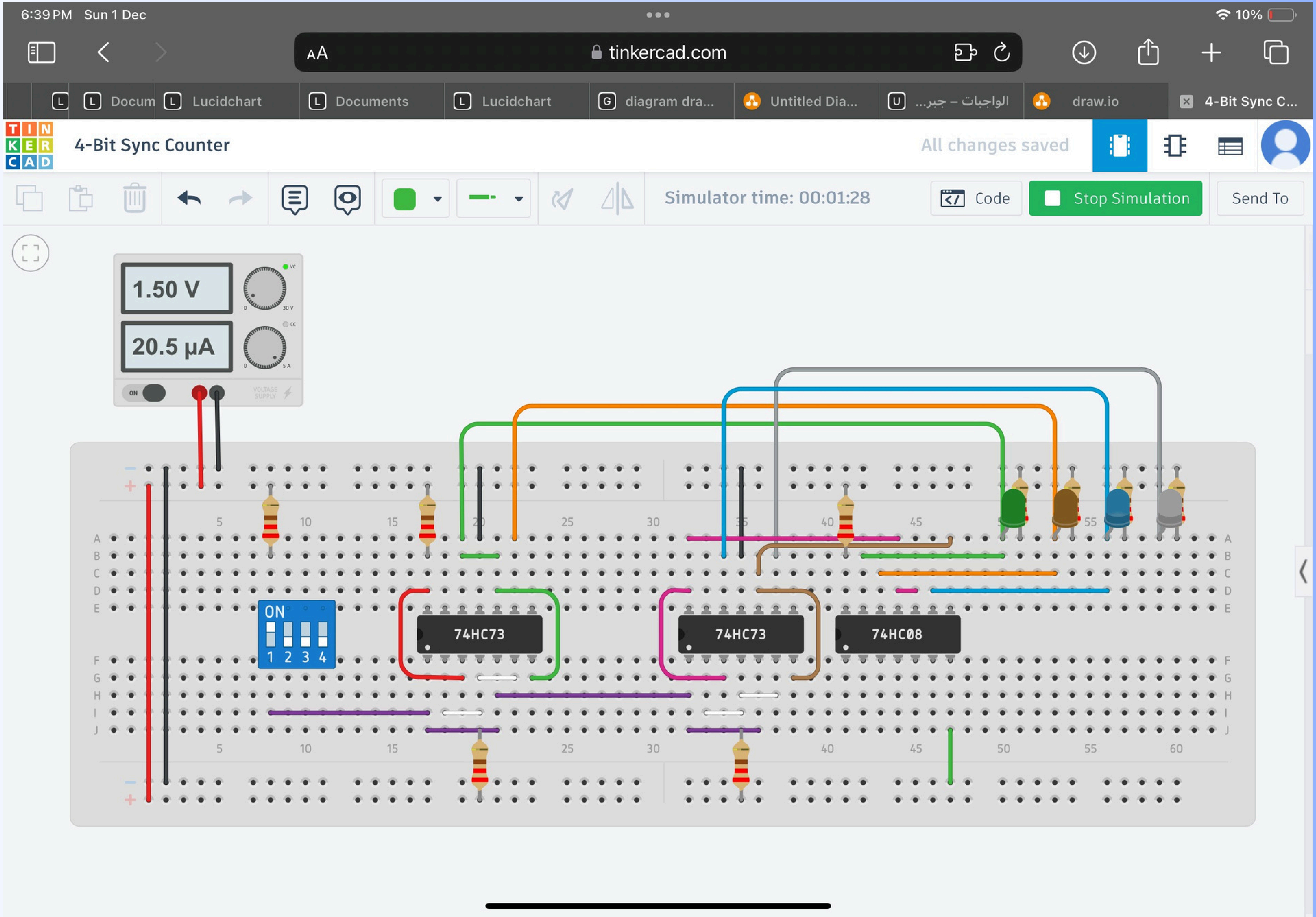
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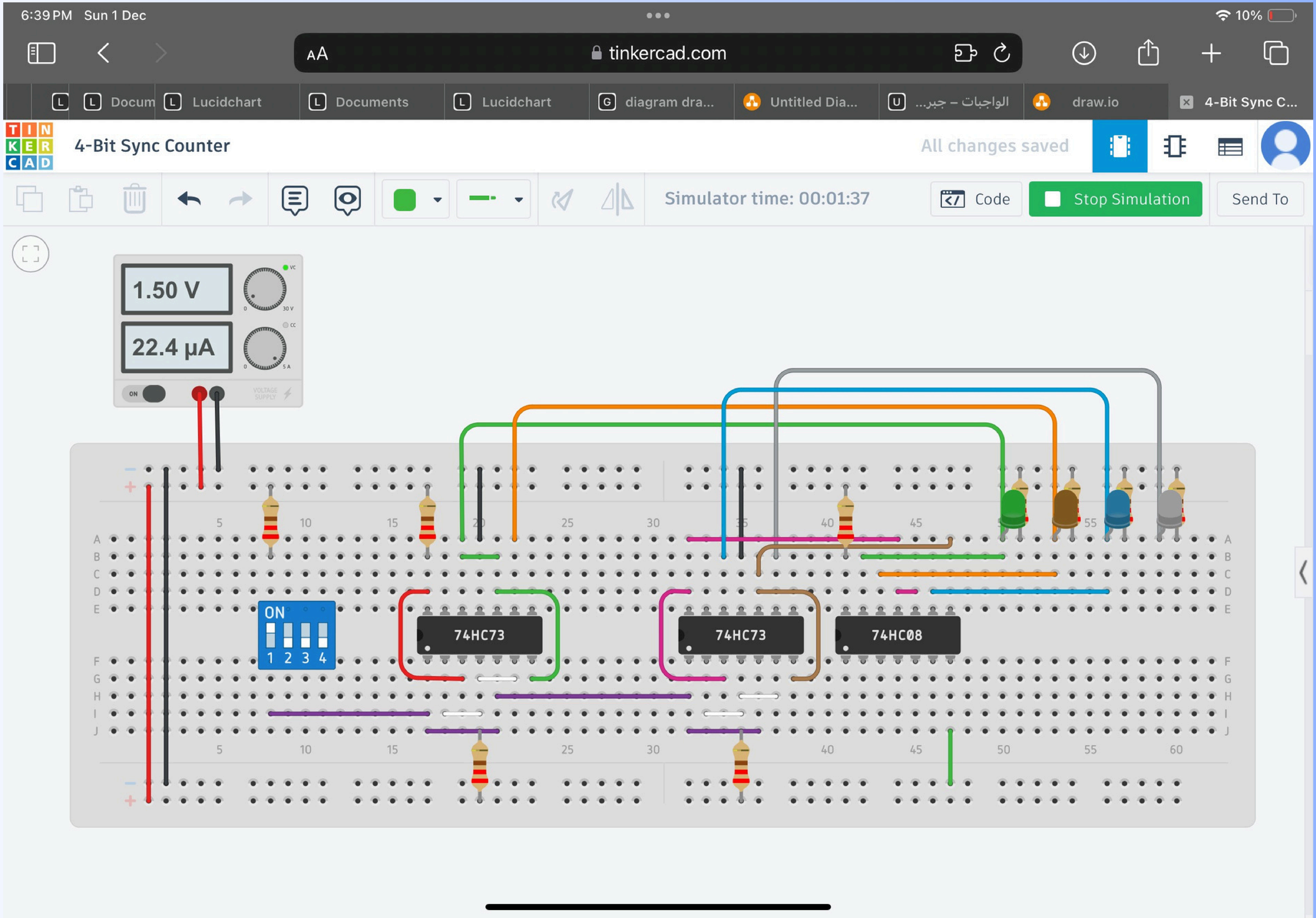
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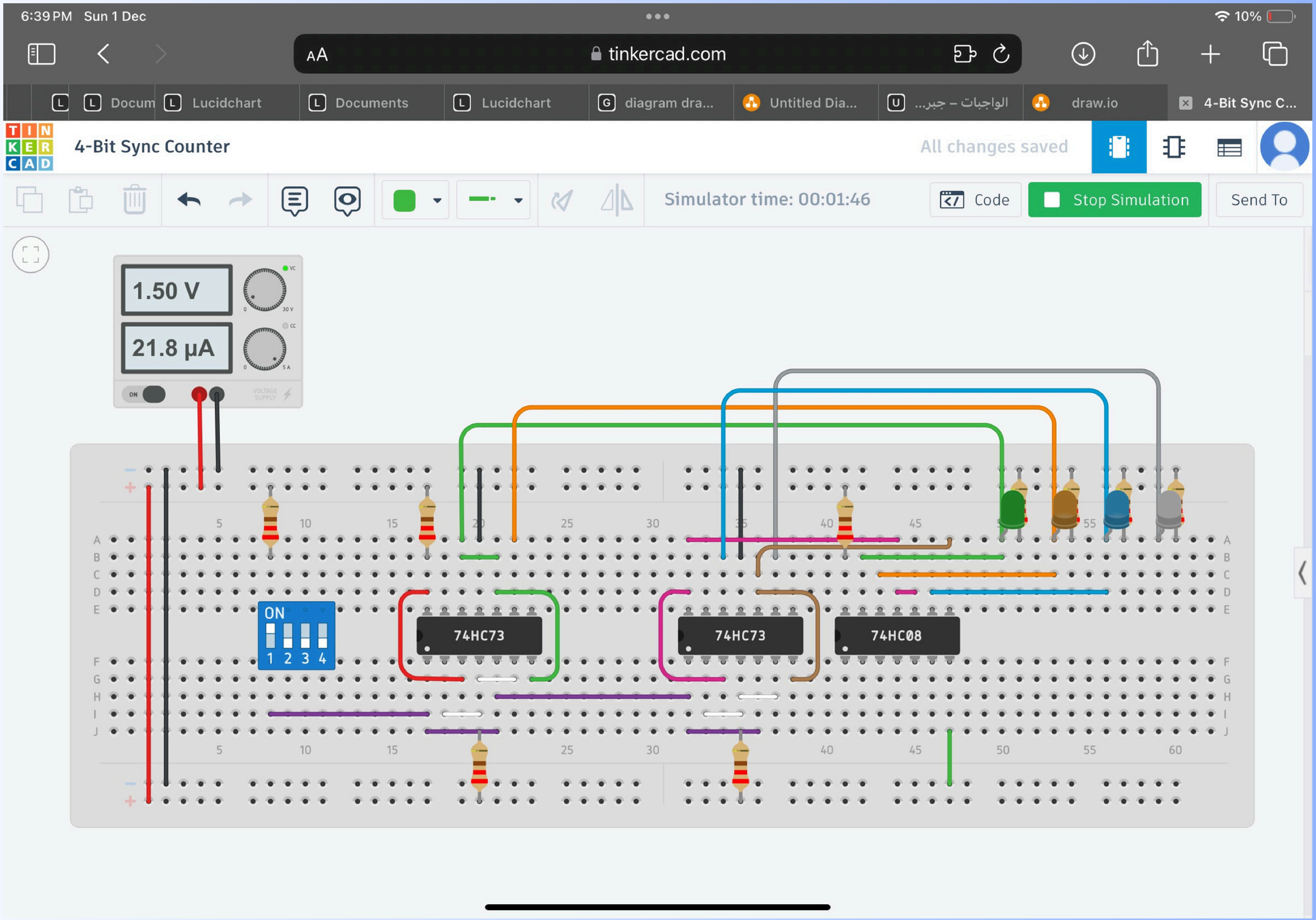
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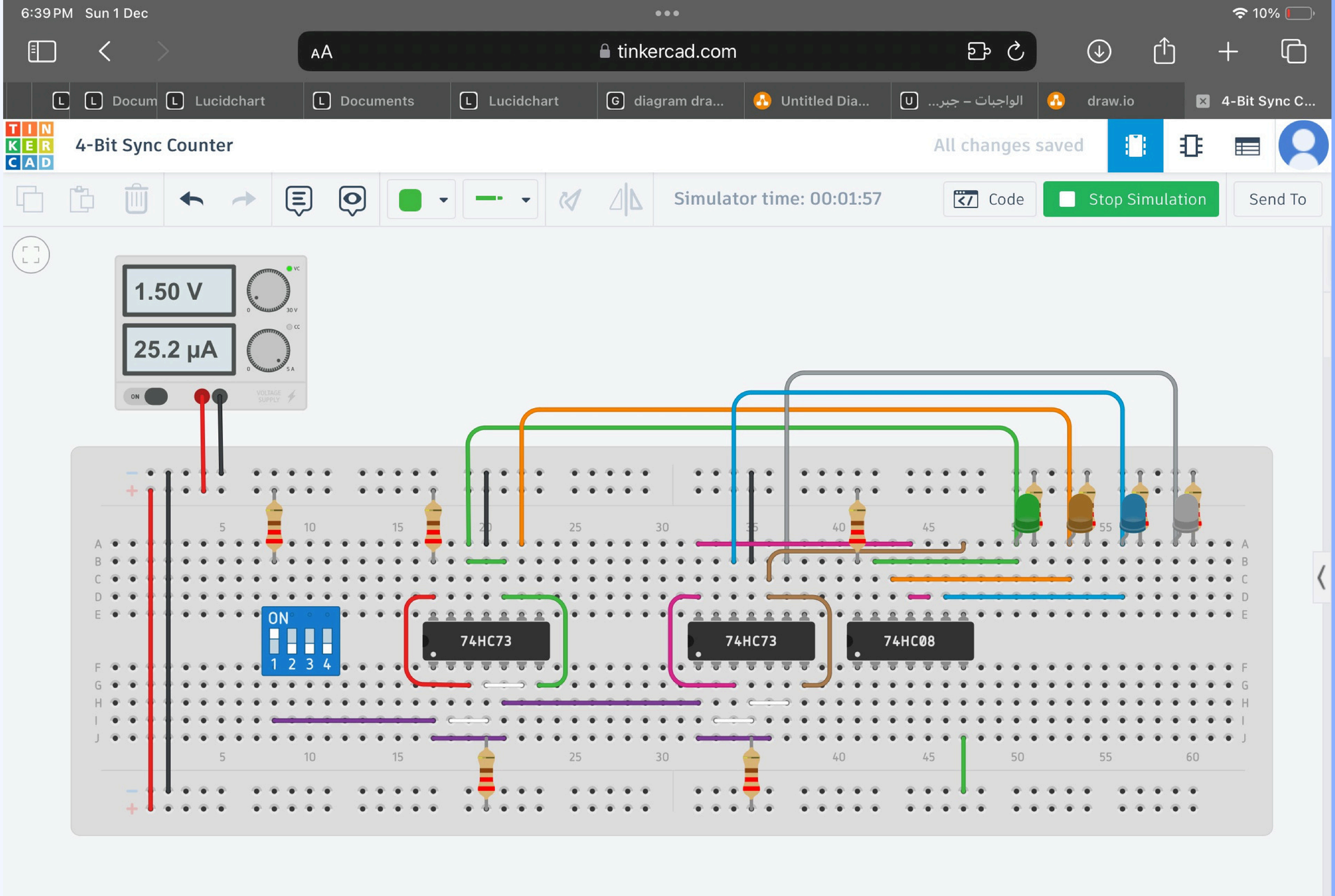
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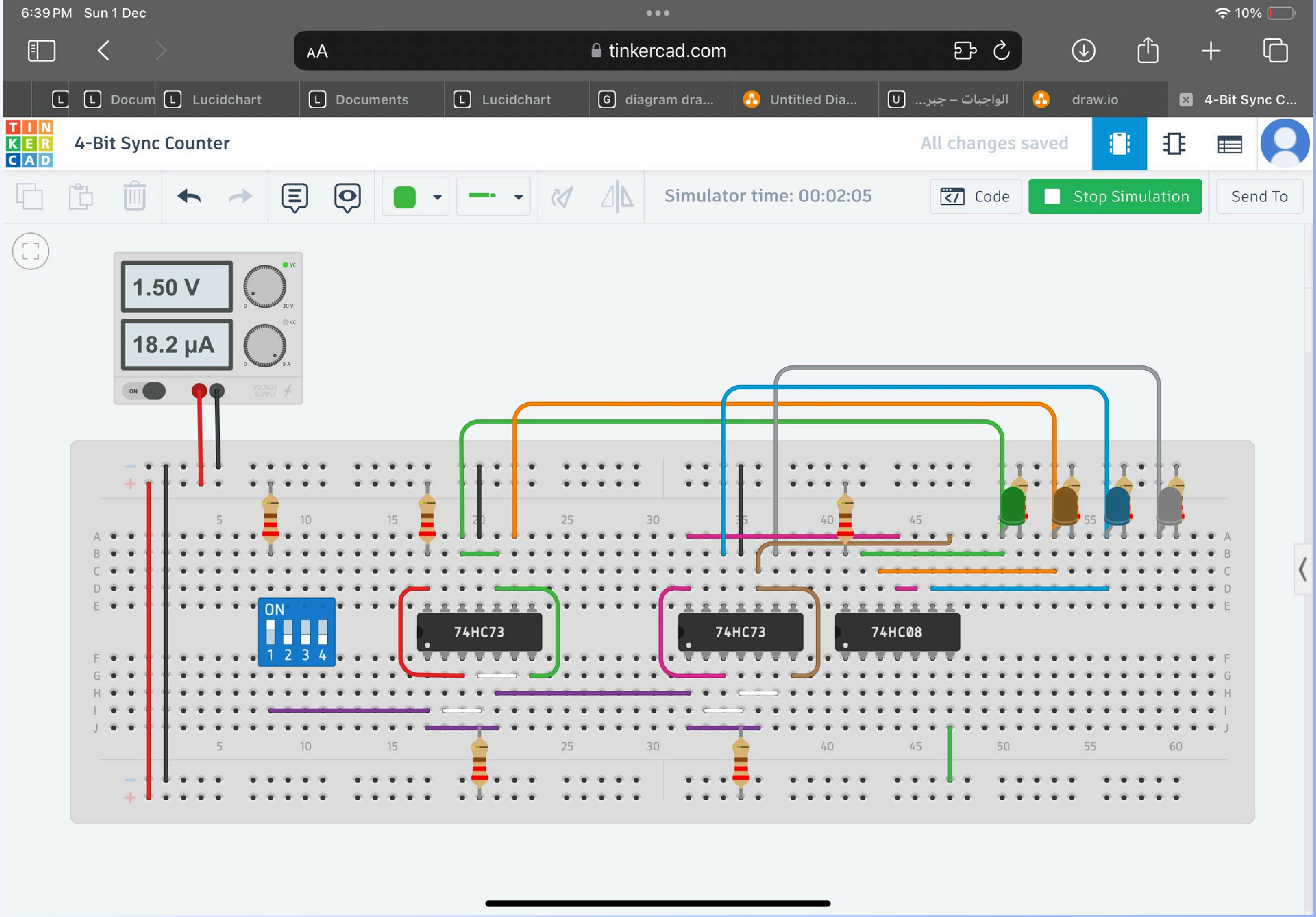
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74HC73
74HC08

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# THANK YOU

| Name | ID | Tasks |
|---|---|---|
| Leen Kharraz | 2412099 | Q1 |
| Wateen Alharthy | 2413523 | Q2 |
| Sarah Alfowzan | 2410916 | Q3 |
| All | All | Circuit |